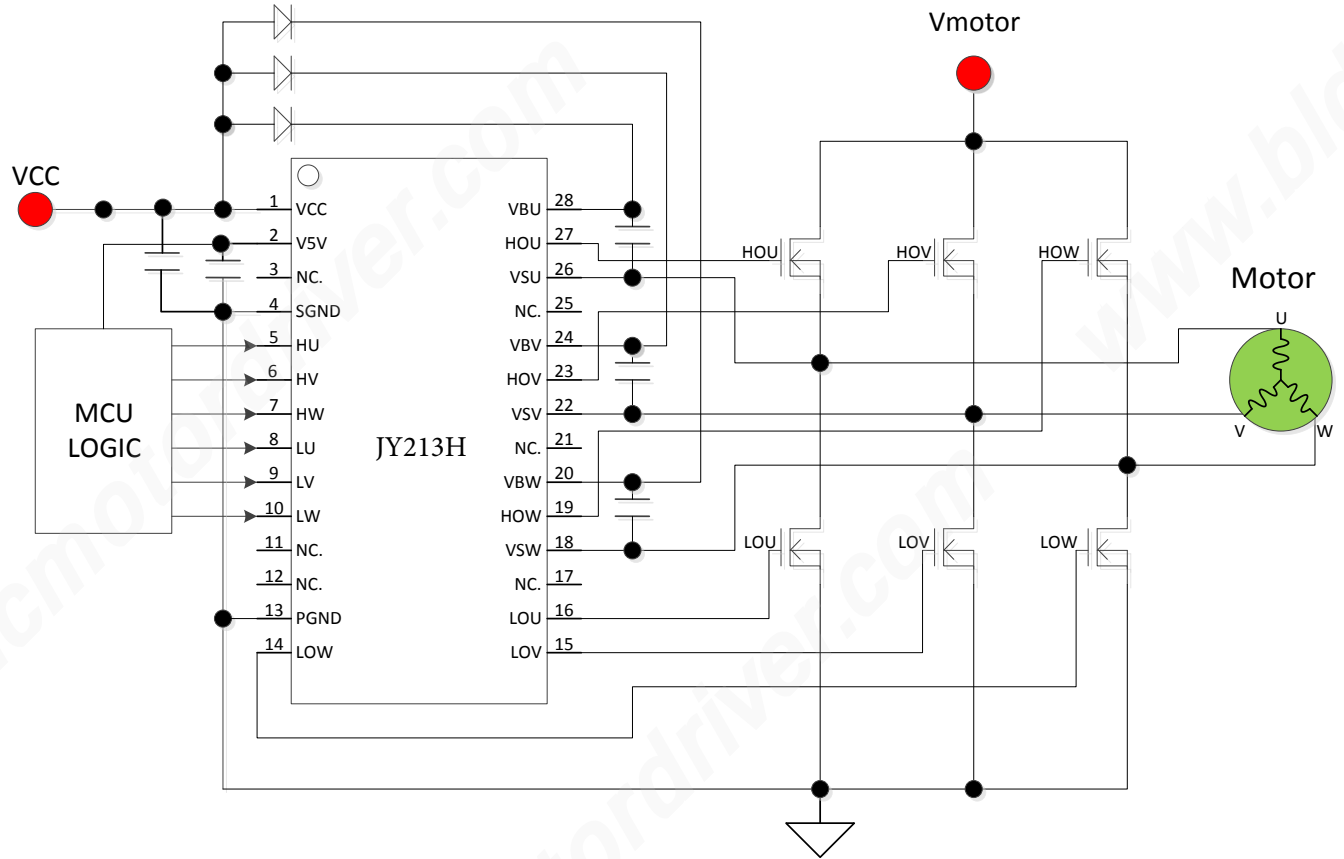


## FEATURES

- Integrated 600V half-bridge high side driver
- Driver up to 3-phase half-bridge gates
- Built-in deadtime control
- Shoot-through protection
- Under voltage lockout for VCC and VBS
- 3.3V, 5V, 15V input logic Compatible
- Built-in input filter
- -40°C to 125°C operating range
- Common-Mode dv/dt Noise Canceling Circuit

- 3-phase Motor Inverter Driver
- Air Condition
- Washing Machines

# TYPICAL APPLICATION CIRCUIT

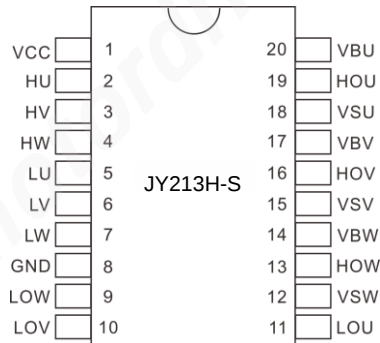


## ORDER INFORMATION

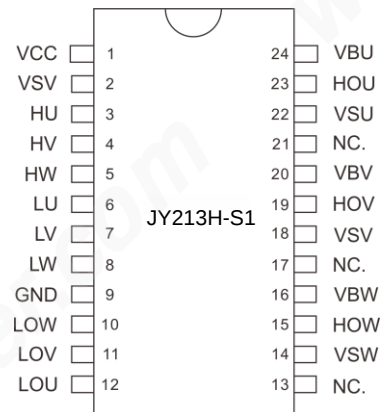
| Valid Part Number | Package Type        | Top Code  |
|-------------------|---------------------|-----------|
| JY213H-S          | 20-PIN, SOP, 300mil | JY213H-S  |
| JY213H-S1         | 24-PIN, SOP, 300mil | JY213H-S1 |
| JY213H-S2         | 28-PIN, SOP, 300mil | JY213H-S2 |

## PIN CONFIGURATION

### 20-PIN



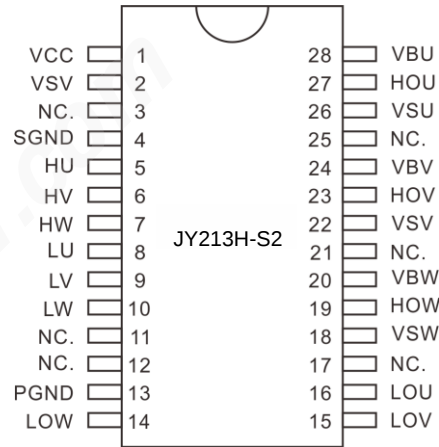
### 24-PIN



## PIN DESCRIPTION

| Pin Name | Description                                             | Pin No. |       |
|----------|---------------------------------------------------------|---------|-------|
|          |                                                         | SOP20   | SOP24 |
| VCC      | Logic and low-side gate drivers power supply voltage    | 1       | 1     |
| V5V      | 5V LDO output                                           |         | 2     |
| HU       | Logic input for high-side gate U-phase driver           | 2       | 3     |
| HV       | Logic input for high-side gate V-phase driver           | 3       | 4     |
| HW       | Logic input for high-side gate W-phase driver           | 4       | 5     |
| LU       | Logic input for low-side gate U-phase driver            | 5       | 6     |
| LV       | Logic input for low-side gate V-phase driver            | 6       | 7     |
| LW       | Logic input for low-side gate W-phase driver            | 7       | 8     |
| GND      | Logic ground and low-side gate drivers ground           | 8       | 9     |
| LOW      | Low-side gate driver W-phase output                     | 9       | 10    |
| LOV      | Low-side gate driver V-phase output                     | 10      | 11    |
| LOU      | Low-side gate driver U-phase output                     | 11      | 12    |
| NC.      | Not Connected                                           |         | 13    |
| VSW      | High-side driver W-phase floating supply offset voltage | 12      | 14    |
| HOW      | High-side driver W-phase gate driver output             | 13      | 15    |
| VBW      | High-side driver W-phase floating supply                | 14      | 16    |
| NC.      | Not Connected                                           |         | 17    |
| VSV      | High-side driver V-phase floating supply offset voltage | 15      | 18    |
| HOV      | High-side driver V-phase gate driver output             | 16      | 19    |
| VBV      | High-side driver V-phase floating supply                | 17      | 20    |
| NC.      | Not Connected                                           |         | 21    |
| VSU      | High-side driver U-phase floating supply offset voltage | 18      | 22    |
| HOU      | High-side driver U-phase gate driver output             | 19      | 23    |
| VBU      | High-side driver U-phase floating supply                | 20      | 24    |

## 28-PIN



## PIN DESCRIPTION

| Pin Name | Description                                             | Pin No. |
|----------|---------------------------------------------------------|---------|
| VCC      | Logic and low-side gate drivers power supply voltage    | 1       |
| V5V      | 5V LDO output                                           | 2       |
| NC.      | Not Connected                                           | 3       |
| SGND     | Logic ground                                            | 4       |
| HU       | Logic input for high-side gate U-phase driver           | 5       |
| HV       | Logic input for high-side gate V-phase driver           | 6       |
| HW       | Logic input for high-side gate W-phase driver           | 7       |
| LU       | Logic input for low-side gate U-phase driver            | 8       |
| LV       | Logic input for low-side gate V-phase driver            | 9       |
| LW       | Logic input for low-side gate W-phase driver            | 10      |
| NC.      | Not Connected                                           | 11      |
| NC.      | Not Connected                                           | 12      |
| PGND     | Low-side gate drivers ground                            | 13      |
| LOW      | Low-side gate driver W-phase output                     | 14      |
| LOV      | Low-side gate driver V-phase output                     | 15      |
| LOU      | Low-side gate driver U-phase output                     | 16      |
| NC.      | Not Connected                                           | 17      |
| VSW      | High-side driver W-phase floating supply offset voltage | 18      |
| HOW      | High-side driver W-phase gate driver output             | 19      |
| VBW      | High-side driver W-phase floating supply                | 20      |
| NC.      | Not Connected                                           | 21      |
| VSV      | High-side driver V-phase floating supply offset voltage | 22      |
| HOV      | High-side driver V-phase gate driver output             | 23      |
| VBV      | High-side driver V-phase floating supply                | 24      |
| NC.      | Not Connected                                           | 25      |
| VSU      | High-side driver U-phase floating supply offset voltage | 26      |
| HOU      | High-side driver U-phase gate driver output             | 27      |
| VBU      | High-side driver U-phase floating supply                | 28      |

## FUNCTION DESCRIPTION

### LOW SIDE POWER SUPPLY ( $V_{CC}$ , $GND$ ( $SGND$ , $PGND$ ))

$V_{CC}$  is the low side supply and it provides power to both input logic and low side output power stage. In JY213H-S2, input logic is referenced to  $SGND$  as well as the under-voltage detection circuit. Output power stage is referenced to  $PGND$ .  $PGND$  ground is floating respect to  $SGND$  ground with a recommended range of operation of  $\pm 5V$ , which guarantees enough margin of gate to source voltage,  $V_{GS}$ , to driver power devices such as power MOSFET. The built-in under-voltage lockout circuit enables the device to operate at sufficient power on when a typical  $V_{CC}$  supply voltage higher than  $V_{CCUV+} = 9.5$  is present, shown as FIG1. The IC shuts down all the gate drivers outputs, when the  $V_{CC}$  supply voltage is below  $V_{CCUV-} = 8.8$  V, shown as FIG1. This prevents the external power devices from extremely low gate voltage levels during on-state and therefore from excessive power dissipation.

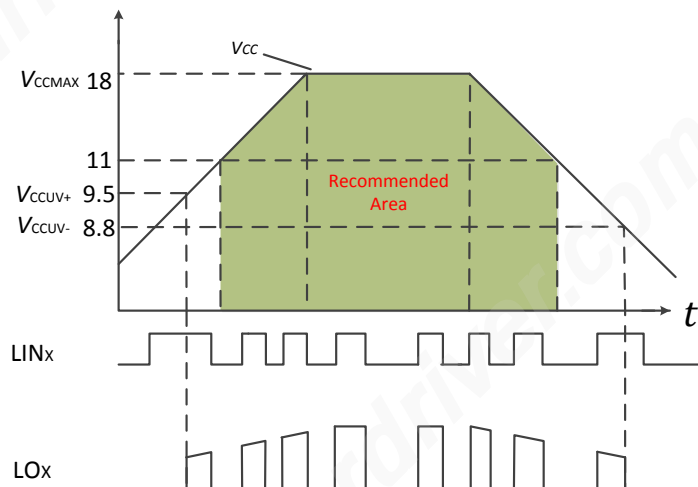


FIG.1 VCC supply UVLO operating area

### HIGH SIDE POWER SUPPLY ( $V_{BU-VSU}$ , $V_{BV-VSV}$ , $V_{BW-VSW}$ )

$VB$  to  $VS$  is the high side supply voltage. The totally high side circuitry can float with respect to  $SGND$  following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to  $V_{CC}$ , and it can be powered with small bootstrap capacitors.

The device operating area as a function of the supply voltage is given in Figure2.

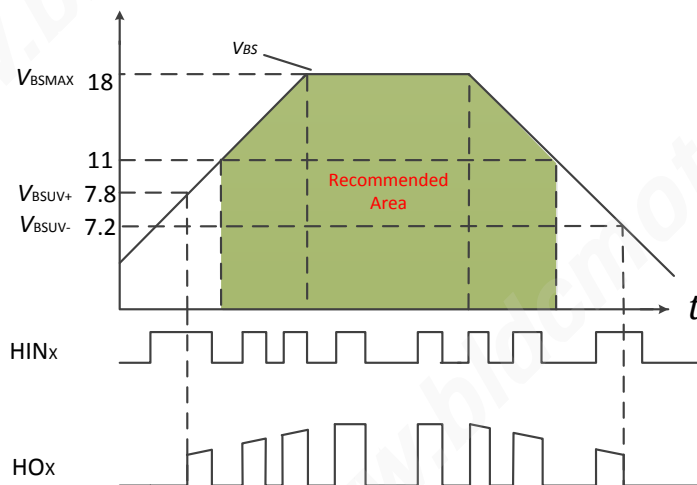


FIG.2 VBS supply UVLO operating area

## LOW SIDE AND HIGH CONTROL INPUT LOGIC (HU, V, W / LU, V, W)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and advanced noise filter provide beneficial noise rejection to short input pulses. An internal pull-down resistor of about 200k $\Omega$  (positive logic) pre-biases each input during VCC supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 400ns.

## SHOOT-THROUGH PREVENTION

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 3 shows how this prevention circuitry prevents both the high- and low-side switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “high”, the both driver outputs are pulled down “low” to shutdown two power devices in the same bridge.

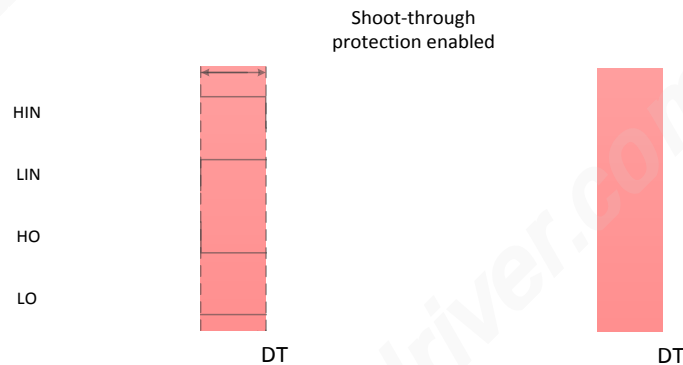


FIG.3 Shoot-through prevention

## DEAD TIME

The IC features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 4 illustrates the dead time period and the relationship between the output gate signals.

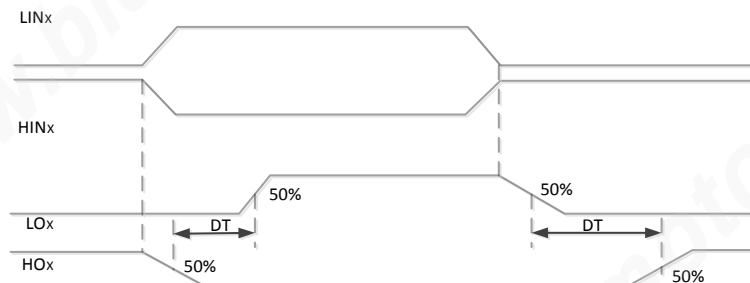


FIG.4 Dead Time

## GATE DRIVER (HOU, V, W, LOU, V, W)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power devices such as IGBT and MOSFET. Low side outputs (i.e. LOU, V, W) are state triggered by the respective inputs, while high side outputs (i.e. HOU, V, W) are only changed at the edge of the respective inputs. In particular, after releasing from an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC supply, the low side outputs can directly switch to the state of their respective inputs and don't suffer from the trouble as high side driver.

## ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC SGND unless otherwise stated in the table.

| Parameter                            | Symbol                         | Min.                | Max.                | Units |
|--------------------------------------|--------------------------------|---------------------|---------------------|-------|
| High-side floating supply voltage    | $V_{B.U.V.W}$                  | -0.3                | 600                 | V     |
| High-side offset voltage             | $V_{S.U.V.W}$                  | $V_{B.U.V.W} - 18$  | $V_{B.U.V.W} + 0.3$ |       |
| High-side gate driver output voltage | $V_{HO.U.V.W}$                 | $V_{S.U.V.W} - 0.3$ | $V_{S.U.V.W} + 0.3$ |       |
| Low-side gate driver output voltage  | $V_{LO.U.V.W}$                 | PGND-0.3            | $V_{CC} + 0.3$      |       |
| Logic input voltage                  | $V_{H.U.V.W}$<br>$V_{L.U.V.W}$ | -0.3                | 20                  |       |
| Low-side supply voltage              | $V_{CC}$                       | -0.3                | 20                  |       |
| Logic gate driver return             | PGND                           | $V_{CC} - 18$       | $V_{CC} + 0.3$      | V/ns  |
| Allowable Offset Voltage Slew Rate   | dV/dt                          |                     | 40                  |       |
| Junction temperature                 | $T_J$                          | -40                 | +125                |       |
| Storage temperature                  | $T_S$                          | -50                 | +150                | °C    |

## RECOMMENDED OPERATING CONDITIONS

| Parameter                                       | Symbol                         | Min.       | Typ. | Max.       | Units |
|-------------------------------------------------|--------------------------------|------------|------|------------|-------|
| Low-side supply voltage                         | $V_{CC}$                       | 11         | -    | 18         | V     |
| High-side Floating Supply Offset Voltage(note1) | $V_{S.U.V.W}$                  | $V_B - 18$ | -    | $V_B - 11$ |       |
| High-side Floating Supply Voltage               | $V_{B.U.V.W}$                  | -8         | -    | 600        |       |
| High-side gate driver output voltage            | $V_{HO.U.V.W}$                 | $V_S$      | -    | $V_B$      |       |
| Low-side gate driver output voltage             | $V_{LO.U.V.W}$                 | PGND       | -    | $V_{CC}$   |       |
| Logic gate driver return                        | PGND                           | -3         |      | 3          |       |
| Logic input voltage                             | $V_{H.U.V.W}$<br>$V_{L.U.V.W}$ | 0          | -    | 5          |       |
| IC operating Junction temperature               | $T_J$                          | -40        | -    | +125       | °C    |

Note1: For  $V_{BS}=12V$ , normal Logic operation for  $V_S$  of -8 V to 600 V. The parameter is only guaranteed by design.

# STATIC ELECTRICAL CHARACTERISTICS

(VCC-SGND) = (VB-VS)=12V. T<sub>AMB</sub>=25°C unless otherwise specified. The V<sub>IN</sub>, V<sub>TH</sub> and I<sub>IN</sub> Parameters are reference to SGND and are applicable to all six channels. The V<sub>O</sub> and I<sub>O</sub> parameters are referenced to respective V<sub>S</sub> and PGND and are applicable to the respective output leads. The V<sub>CCUV</sub> parameters are referenced to SGND. The V<sub>BSUV</sub> parameters are referenced to V<sub>S</sub>.

| Parameter                                                                  | Symbol               | Test Conditions                                             | Min. | Typ. | Max. | Unit |
|----------------------------------------------------------------------------|----------------------|-------------------------------------------------------------|------|------|------|------|
| Low Side Power Supply Characteristics                                      |                      |                                                             |      |      |      |      |
| VCC quiescent current in UVLO mode                                         | I <sub>QVCC</sub>    | V <sub>H.U.V.W</sub><br>=V <sub>L.U.V.W</sub> =0 or 5V,     | 200  | 350  | 500  | μA   |
| VCC operating Vcc supply current                                           | I <sub>VCCOP</sub>   | f <sub>L.U.V.W</sub> =20k,<br>f <sub>H.U.V.W</sub> =20k,    | -    | 1200 | -    |      |
| VCC supply under-voltage positive going threshold                          | V <sub>CCUV+</sub>   |                                                             | 8.0  | 9.5  | 11.0 | V    |
| VCC supply under-voltage negative going threshold                          | V <sub>CCUV-</sub>   |                                                             | 7.3  | 8.8  | 10.3 |      |
| V <sub>CC</sub> supply under-voltage lockout hysteresis                    | V <sub>CCHYS</sub>   |                                                             | -    | 0.7  | -    |      |
| High Side Floating Power Supply Characteristics                            |                      |                                                             |      |      |      |      |
| High side VBS supply under-voltage positive going threshold                | V <sub>BSUV+</sub>   |                                                             | 6.8  | 7.8  | 8.8  | V    |
| High side VBS supply under-voltage negative going threshold                | V <sub>BSUV-</sub>   |                                                             | 6.2  | 7.2  | 8.2  |      |
| High side VBS supply under-voltage lockout hysteresis                      | V <sub>BSUVHYS</sub> |                                                             | -    | 0.6  | -    |      |
| High side VBS quiescent current in UVLO mode                               | I <sub>QBS</sub>     | V <sub>BS</sub> =12V                                        | 35   | 54   | 75   | μA   |
| Offset supply leakage current                                              | I <sub>LK</sub>      | V <sub>B</sub> =V <sub>S</sub> =600V<br>V <sub>CC</sub> =0V | -    | -    | 1    |      |
| Gate Driver Output Section                                                 |                      |                                                             |      |      |      |      |
| High Side Output High Short-Circuit Pulse Current                          | I <sub>HO+</sub>     | V <sub>HO</sub> =V <sub>S</sub> =0                          | -    | 160  | -    | mA   |
| High Side Output Low Short-Circuit Pulse Current                           | I <sub>HO-</sub>     | V <sub>HO</sub> =V <sub>B</sub> =12V                        | -    | 340  | -    |      |
| Low Side Output High Short-Circuit Pulse Current                           | I <sub>LO+</sub>     | V <sub>LO</sub> =PGND=0                                     | -    | 160  | -    |      |
| Low Side Output Low Short-Circuit Pulse Current                            | I <sub>LO-</sub>     | V <sub>LO</sub> =V <sub>CC</sub> =12V                       | -    | 340  | -    |      |
| Allowable Negative Vs Pin Voltage for HU.V.W Signal Propagation to HOU.V.W | V <sub>SN</sub>      | V <sub>BS</sub> =12V                                        | -    | -10  | -8   | V    |
| Logic Input Section                                                        |                      |                                                             |      |      |      |      |
| Logic"1" Input voltage HU.V.W and LU.V.W                                   | V <sub>IH</sub>      |                                                             | 2.8  | -    | -    | V    |
| Logic"0" Input voltage HU.V.W and LU.V.W                                   | V <sub>IL</sub>      |                                                             | -    | -    | 0.8  |      |
| Input positive going threshold                                             | V <sub>IN,TH+</sub>  |                                                             | -    | 2.0  | -    |      |
| Input negative going threshold                                             | V <sub>IN,TH-</sub>  |                                                             | -    | 1.5  | -    |      |
| Logic "1" Input bias current                                               | I <sub>IN+</sub>     | V <sub>IN</sub> =5V                                         | -    | 25   | -    | uA   |
| Logic "0" Input bias current                                               | I <sub>IN-</sub>     | V <sub>IN</sub> =0                                          | -    | 0    | -    |      |
| LDO Characteristic (Only for JY213H-S1 and JY213H-S2)                      |                      |                                                             |      |      |      |      |
| Output Voltage                                                             | V <sub>LDO</sub>     | VCC=12V                                                     | 4.5  | 5    | 5.5  | V    |
| Output Current                                                             | I <sub>LDO</sub>     |                                                             | -    | 20   | 30   | mA   |

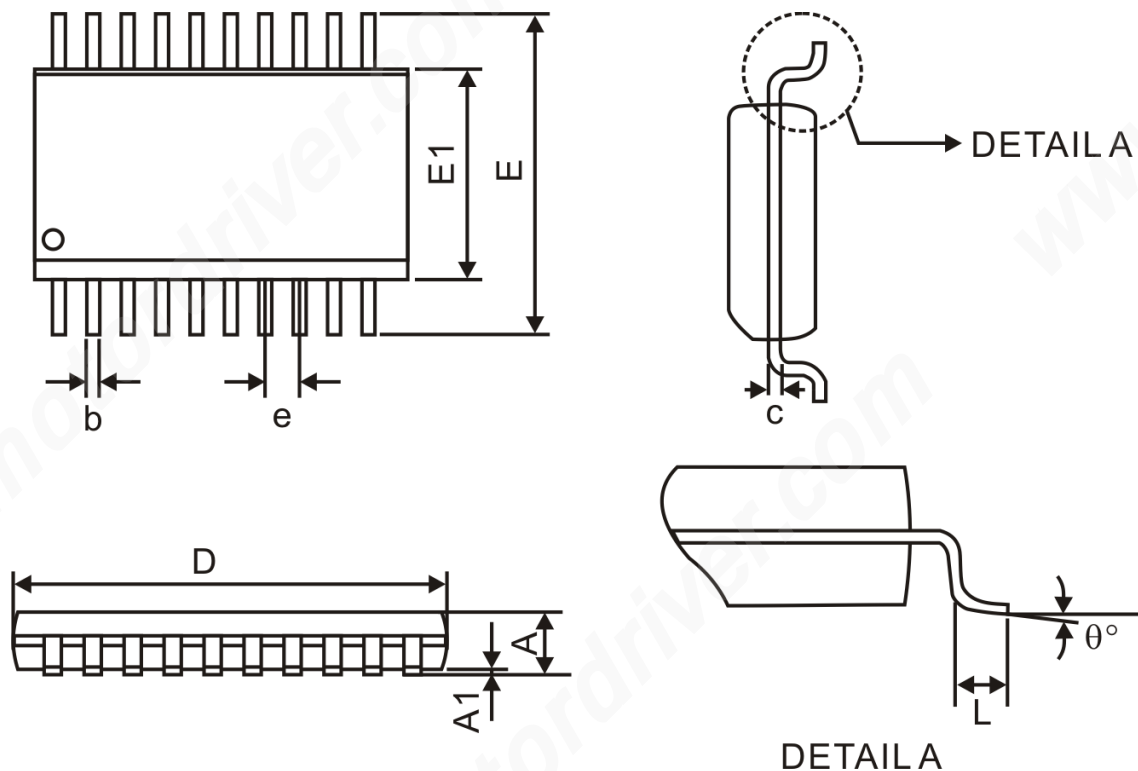
## DYNAMIC ELECTRICAL CHARACTERISTICS

(VCC-SGND) = (VB-VS) = 12V,  $V_{S.U.V.W} = \text{SGND} = \text{PGND}$ , and  $C_{\text{load}} = 1\text{nF}$  unless otherwise specified,  $T_{\text{AMB}} = 25^{\circ}\text{C}$ .

| Parameter                            | Symbol              | Test Conditions                                                                        | Min. | Typ. | Max. | Unit |
|--------------------------------------|---------------------|----------------------------------------------------------------------------------------|------|------|------|------|
| Turn-On propagation delay            | $t_{\text{ON}}$     | $V_{\text{H.U.V.W}}$ or $V_{\text{L.U.V.W}} = 5\text{V}$ ,<br>$V_{\text{S.U.V.W}} = 0$ | 300  | 510  | 700  | ns   |
| Turn-Off Propagation delay           | $t_{\text{OFF}}$    | $V_{\text{H.U.V.W}}$ or $V_{\text{L.U.V.W}} = 0$ ,<br>$V_{\text{S.U.V.W}} = 0$         | 300  | 570  | 700  |      |
| Turn-On Rise time                    | $t_{\text{R}}$      | $V_{\text{H.U.V.W}}$ or $V_{\text{L.U.V.W}} = 5\text{V}$ ,<br>$V_{\text{S.U.V.W}} = 0$ | -    | 90   | -    |      |
| Turn-Off Fall time                   | $t_{\text{F}}$      | $V_{\text{H.U.V.W}}$ or $V_{\text{L.U.V.W}} = 0$ ,<br>$V_{\text{S.U.V.W}} = 0$         | -    | 40   | -    |      |
| Input Filtering Time                 | $t_{\text{FLT,IN}}$ |                                                                                        | -    | 400  | -    |      |
| Dead Time                            | DT                  |                                                                                        | 150  | 230  | 310  |      |
| Dead-Time Matching(All Six Channels) | MDT                 |                                                                                        | -    | -    | 100  |      |
| Delay Matching(All Six Channels)     | MT                  |                                                                                        | -    | -    | 150  |      |
| Output Pulse-Width Matching          | PM                  | $PW_{\text{IN}} = 10\mu\text{s}$ ,<br>$PM = PW_{\text{OUT}} - PW_{\text{IN}}$          | -    | -    | 100  |      |

# PACKAGE INFORMATION

20-PIN, SOP, 300MIL

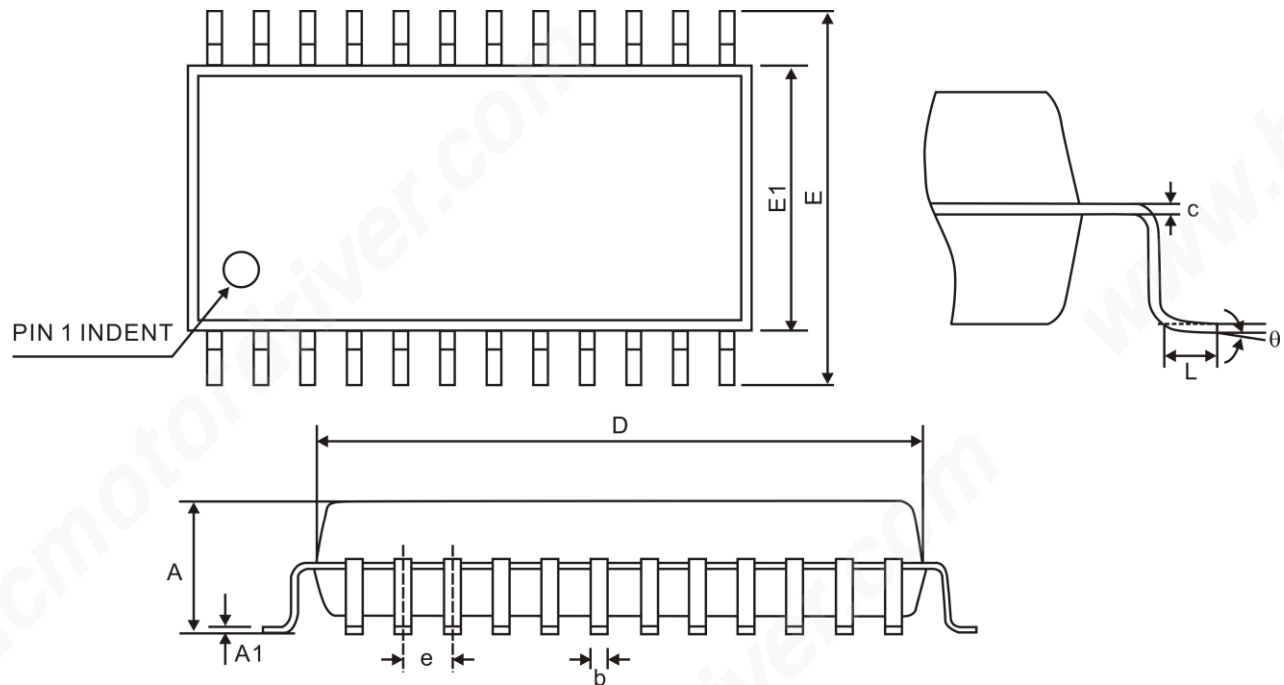


| Symbol | Min.       | Typ. | Max. |
|--------|------------|------|------|
| A      | -          | -    | 2.65 |
| A1     | 0.10       | -    | 0.30 |
| b      | 0.31       | -    | 0.51 |
| c      | 0.20       | -    | 0.33 |
| e      | 1.27 BSC.  |      |      |
| D      | 12.80 BSC. |      |      |
| E      | 10.30 BSC. |      |      |
| E1     | 7.50 BSC.  |      |      |
| L      | 0.40       | -    | 1.27 |
| θ      | 0°         | -    | 8°   |

Notes:

1. Refer to JEDEC MS-013 AC.
2. Unit: mm.

## 24-PIN, SOP, 300MIL

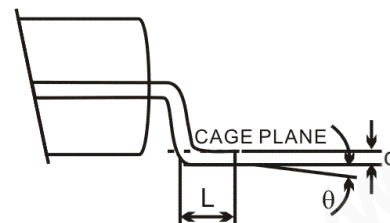
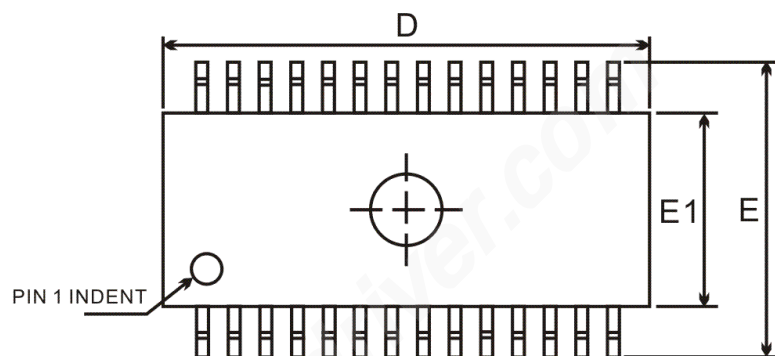


| Symbol | Min.       | Typ. | Max. |
|--------|------------|------|------|
| A      | -          | -    | 2.65 |
| A1     | 0.10       | -    | 0.30 |
| b      | 0.31       | -    | 0.51 |
| c      | 0.20       | -    | 0.33 |
| e      | 1.27 BSC.  |      |      |
| D      | 15.40 BSC. |      |      |
| E      | 10.30 BSC. |      |      |
| E1     | 7.50 BSC.  |      |      |
| L      | 0.40       | -    | 1.27 |
| θ      | 0°         | -    | 8°   |

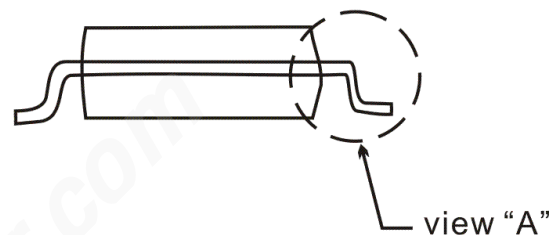
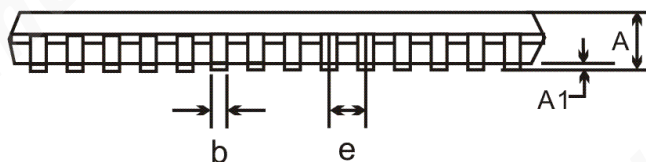
Notes:

1. All controlling dimensions are in millimeter.
2. Refer to JEDEC MS-013 AD.

## 28-PIN, SOP 300MIL



view "A"



view "A"

| Symbol   | Min.     | Nom. | Max. |
|----------|----------|------|------|
| A        | -        | -    | 2.65 |
| A1       | 0.10     | -    | 0.30 |
| b        | 0.31     | -    | 0.51 |
| c        | 0.20     | -    | 0.33 |
| e        | 1.27BSC  |      |      |
| D        | 17.90BSC |      |      |
| E        | 10.30BSC |      |      |
| E1       | 7.50BSC  |      |      |
| L        | 0.38     | -    | 1.27 |
| $\theta$ | 0°       | -    | 8°   |

### Notes:

- Controlling dimension is Millimeter.
- All dimensions refer to JEDEC standard MS-013 AE.